SELECTED PUBLICATIONS of the DSP DESIGN GROUP

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1993

[1] A. Kalavade, and E.A. Lee, "A Hardware/Software Codesign Methodology for DSP Applications," *to appear, IEEE Design and Test*, September 1993.

[2] S. Bhattacharrya, J. Buck, S.-H. Ha, E. A. Lee, "Generating Compact Code from Dataflow Specifications of Multirate DSP Algorithms," UCB/ERL Technical Report M93/36, May 21, 1993.

[3] S. Bhattacharrya and E. A. Lee, "Looped Schedules for Dataflow Descriptions of Multi rate DSP Algorithms," UCB/ERL Technical Report, May 21, 1993.

[4] S. Bhattacharyya and E. A. Lee, "Scheduling Synchronous Dataflow Graphs for Efficient Looping," **to appear** in *J. of VLSI Signal Processing,* 1992.

[5] J. Pino, S. Ha, E. Lee, J. Buck, "Software Synthesis for DSP Using Ptolemy", invited paper in the *Journal on VLSI Signal Processing*, special issue on "Synthesis for DSP", **to appear**.

[6] J. Barry, E. A. Lee, and D. G. Messerschmitt, "Capacity Penalty due to Ideal Zero-Forcing Decision-Feedback Equalization," **to appear** in *IEEE Trans. on Information Theory*, 1993.

[7] J. Buck, S. Ha, E. A. Lee, D. G. Messerschmitt, "Ptolemy: a Framework for Simulating and Prototyping Heterogeneous Systems", **to appear** in *International Journal of Computer Simulation*, special issue on "Simulation Software Development," 1993.

[8] G. C. Sih and E. A. Lee, "Declustering: A New Multiprocessor Scheduling Technique," **to appear** in *IEEE Trans. on Parallel and Distributed Systems,* 1993.

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[13] G. C. Sih and E.A. Lee, "A Compile-Time Scheduling Heuristic for Interconnection-Constrained Heterogeneous Processor Architectures", *IEEE Trans. on Parallel and Distributed Systems,* Vol. 4, No. 2, February, 1993.

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[16] S. Bhattacharyya, Soonhoi Ha, and E. A. Lee, "Single Appearance Schedules for Synchronous Dataflow Programs," Memorandum UCB/ERL M93/4, January 10, 1993.

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[17] Brian Link, *The Waveguide Toolkit*, **MS Report**, EECS Dept., University of California, Berkeley, CA 94720, December, 1992.

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